

Value line, 16-MHz STM8S 8-bit MCU, 8-Kbyte Flash memory, 128-byte data EEPROM, 10-bit ADC, 3 timers, UART, SPI, I<sup>2</sup>C

Datasheet - production data

## Features

### Core

- 16 MHz advanced STM8 core with Harvard architecture and 3-stage pipeline
- Extended instruction set

### Memories

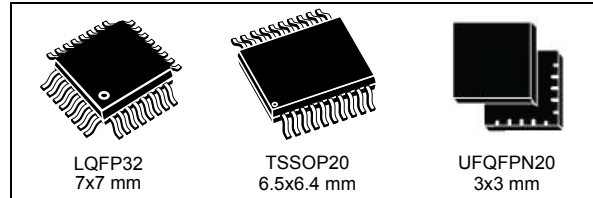
- Program memory: 8 Kbyte Flash memory; data retention 20 years at 55 °C after 100 cycles
- RAM: 1 Kbyte
- Data memory: 128 bytes true data EEPROM; endurance up to 100 k write/erase cycles

### Clock, reset and supply management

- 2.95 V to 5.5 V operating voltage
- Flexible clock control, 4 master clock sources
  - Low-power crystal resonator oscillator
  - External clock input
  - Internal, user-trimmable 16 MHz RC
  - Internal low-power 128 kHz RC
- Clock security system with clock monitor
- Power management
  - Low-power modes (wait, active-halt, halt)
  - Switch-off peripheral clocks individually
  - Permanently active, low-consumption power-on and power-down reset

### Interrupt management

- Nested interrupt controller with 32 interrupts
- Up to 27 external interrupts on 6 vectors



### Timers

- Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
- 16-bit general purpose timer, with 3 CAPCOM channels (IC, OC or PWM)
- 8-bit basic timer with 8-bit prescaler
- Auto wakeup timer
- Window and independent watchdog timers

### Communications interfaces

- UART with clock output for synchronous operation, SmartCard, IrDA, LIN master mode
- SPI interface up to 8 Mbit/s
- I<sup>2</sup>C interface up to 400 Kbit/s

### Analog to digital converter (ADC)

- 10-bit ADC,  $\pm 1$  LSB ADC with up to 5 multiplexed channels, scan mode and analog watchdog

### I/Os

- Up to 28 I/Os on a 32-pin package including 21 high-sink outputs
- Highly robust I/O design, immune against current injection

### Development support

- Embedded single-wire interface module (SWIM) for fast on-chip programming and non-intrusive debugging

# 1 Introduction

This datasheet contains the description of the STM8S003F3/K3 value line features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S and STM8A microcontroller families reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the PM0051 (How to program STM8S and STM8A Flash program memory and data EEPROM).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

## 2 Description

The STM8S003F3/K3 value line 8-bit microcontrollers offer 8 Kbytes of Flash program memory, plus integrated true data EEPROM. They are referred to as low-density devices in the STM8S microcontroller family reference manual (RM0016).

The STM8S003F3/K3 value line devices provide the following benefits: performance, robustness and reduced system cost.

Device performance and robustness are ensured by true data EEPROM supporting up to 100000 write/erase cycles, advanced core and peripherals made in a state-of-the-art technology at 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

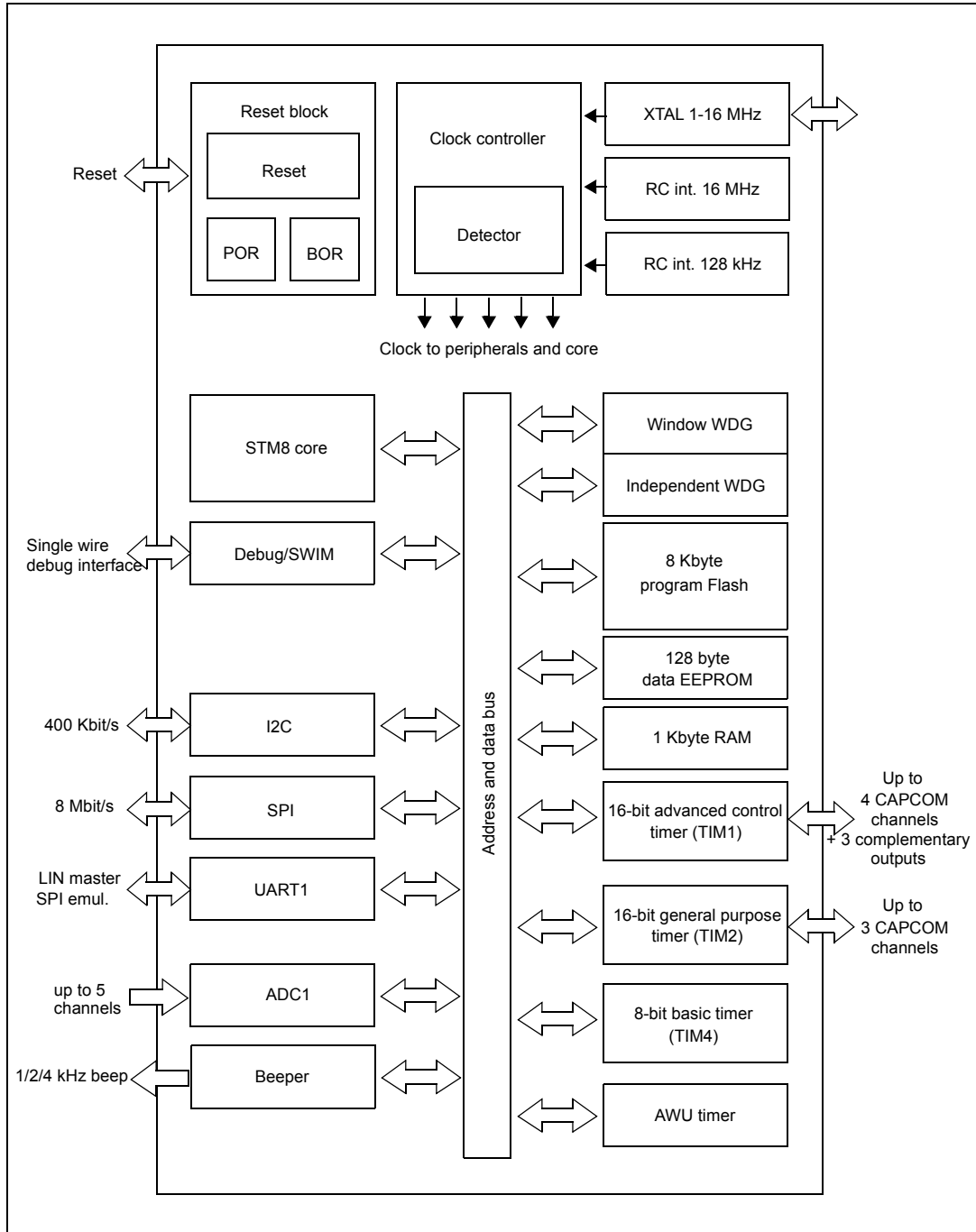
**Table 1. STM8S003F3/K3 value line features**

Features	STM8S003K3	STM8S003F3
Pin count	32	20
Max. number of GPIOs (I/O)	28	16
External interrupt pins	27	16
Timer CAPCOM channels	7	7
Timer complementary outputs	3	2
A/D converter channels	4	5
High-sink I/Os	21	12
Low-density Flash program memory (byte)	8 K	8 K
RAM (byte)	1 K	1 K
True data EEPROM (byte)	128 <sup>(1)</sup>	128 <sup>(1)</sup>
Peripheral set	Multi purpose timer (TIM1), SPI, I2C, UART, Window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4)	

1. Without read-while-write capability.

### 3 Block diagram

Figure 1. STM8S003F3/K3 value line block diagram



## 4 Product overview

The following section intends to give an overview of the basic features of the STM8S003F3/K3 value line functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

### 4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

#### Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

#### Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

#### Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

## 4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

### SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 byte/ms.

### Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

## 4.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 27 external interrupts on six vectors including TLI
- Trap and reset interrupts

## 4.4 Flash program memory and data EEPROM

- 8 Kbyte of Flash program single voltage Flash memory
- 128 byte true data EEPROM
- User option byte area

### Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to modify the content of main program memory and data EEPROM, or to reprogram the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to [Figure 2](#).

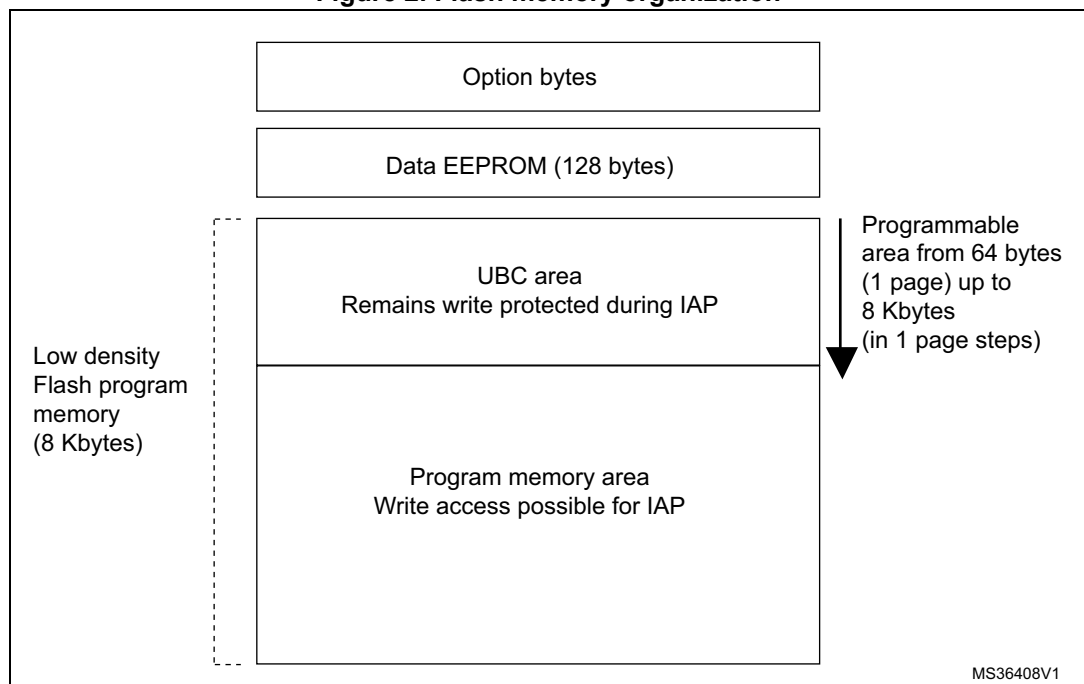
The size of the UBC is programmable through the UBC option byte (*Table 13*), in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: 8 Kbyte minus UBC
- User-specific boot code (UBC): Configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

**Figure 2. Flash memory organization**



**Read-out protection (ROP)**

The read-out protection blocks reading and writing from/to the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

## 4.5 Clock controller

The clock controller distributes the system clock ( $f_{MASTER}$ ) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

### Features

- **Clock prescaler:** To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** Four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK\_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART1	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	Reserved	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I <sup>2</sup> C	PCKEN24	Reserved	PCKEN20	Reserved

## 4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between the lowest power consumption, the fastest start-up time and available wakeup sources.

- **Wait mode:** In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active halt mode with regulator on:** In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active halt mode with regulator off:** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode:** In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

## 4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

### Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: at 16 MHz CPU clock the time-out period can be adjusted between 75  $\mu$ s up to 64 ms.
2. Refresh out of window: the down-counter is refreshed before its value is lower than the one stored in the window register.

### Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60  $\mu$ s to 1 s.

## 4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration

## 4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

## 4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

## 4.11 TIM2 - 16-bit general purpose timer

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1...32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update

## 4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 3. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchronization/chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

## 4.13 Analog-to-digital converter (ADC1)

STM8S003F3/K3 value line products contain a 10-bit successive approximation A/D converter (ADC1) with up to 5 external multiplexed input channels and the following main features:

- Input voltage range: 0 to  $V_{DDA}$
- Conversion time: 14 clock cycles
- Single and continuous, buffered continuous conversion modes
- Buffer size (10 x 10 bits)
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

*Note:* Additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC\_DRH/ADC\_DRL registers.

## 4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: full feature UART, synchronous mode, SPI master mode, SmartCard mode, IrDA mode, LIN2.1 master capability
- SPI: full and half-duplex, 8 Mbit/s
- I<sup>2</sup>C: up to 400 Kbit/s

### 4.14.1 UART1

#### Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

#### Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s ( $f_{CPU}/16$ ) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

#### Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz ( $f_{CPU}/16$ )

#### LIN master mode

- Emission: generates 13-bit synch. break frame
- Reception: detects 11-bit break frame

### 4.14.2 SPI

- Maximum speed: 8 Mbit/s ( $f_{MASTER}/2$ ) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

### 4.14.3 I<sup>2</sup>C

- I<sup>2</sup>C master features
  - Clock generation
  - Start and stop generation
- I<sup>2</sup>C slave features
  - Programmable I<sup>2</sup>C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

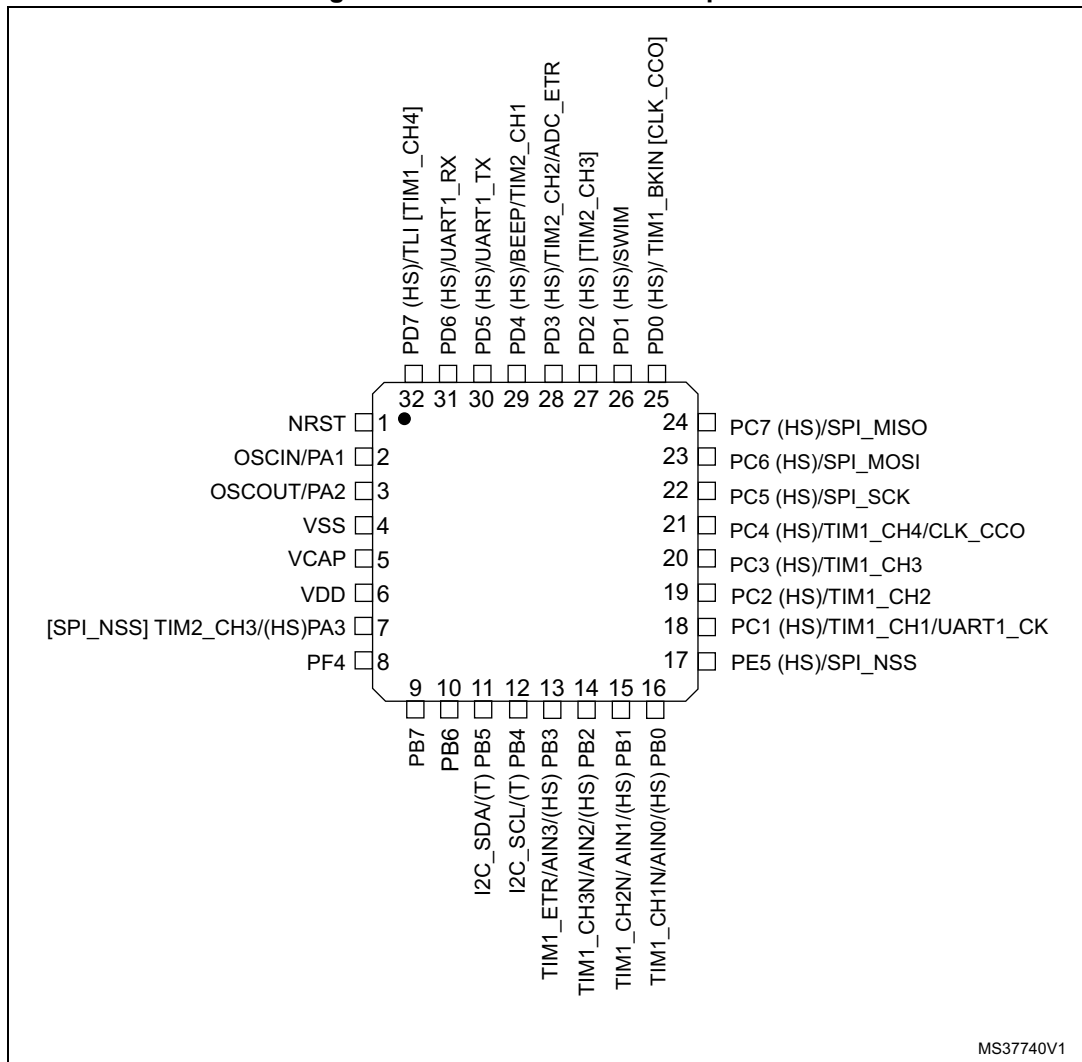
## 5 Pinouts and pin descriptions

**Table 4. Legend/abbreviations for STM8S003F3/K3 pin description tables**

Type	I = input, O = output, S = power supply	
Level	Input	CM = CMOS
	Output	HS = high sink
Output speed	O1 = slow (up to 2 MHz) O2 = fast (up to 10 MHz) O3 = fast/slow programmability with slow as default state after reset O4 = fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold <b>x</b> (pin state after internal reset release) Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

### 5.1 STM8S003K3 LQFP32 pinout and pin description

Figure 3. STM8S003K3 LQFP32 pinout



MS37740V1

Table 5. STM8S003K3 descriptions

LQFP32	Pin name	Type	Input			Output			Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink <sup>(1)</sup>	Speed	OD			
1	NRST	I/O	-	X	-	-	-	-	Reset	-	
2	PA1/OSCIN <sup>(2)</sup>	I/O	X	X	X	-	O1	X	Port A1	Resonator/crystal in	

Table 5. STM8S003K3 descriptions (continued)

LQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink <sup>(1)</sup>	Speed	OD	PP			
3	PA2/OSCOUT	I/O	X	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
4	V <sub>SS</sub>	S	-	-	-	-	-	-	-	Digital ground		-
5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
6	V <sub>DD</sub>	S	-	-	-	-	-	-	-	Digital power supply		-
7	PA3/TIM2_CH3 [SPI_NSS]	I/O	X	X	X	HS	O3	X	X	Port A3	Timer 2 channel 3	SPI master/ slave select [AFR1]
8	PF4	I/O	X	X	-	-	O1	X	X	Port F4	-	-
9	PB7	I/O	X	X	-	-	O1	X	X	Port B7	-	-
10	PB6	I/O	X	X	-	-	O1	X	X	Port B6	-	-
11	PB5/I <sup>2</sup> C_SDA	I/O	X	-	X	-	O1	T <sup>(3)</sup>	-	Port B5	I <sup>2</sup> C data	-
12	PB4/I <sup>2</sup> C_SCL	I/O	X	-	X	-	O1	T <sup>(3)</sup>	-	Port B4	I <sup>2</sup> C clock	-
13	PB3/AIN3 [TIM1_ETR]	I/O	X	X	X	HS	O3	X	X	Port B3	Analog input 3/Timer 1 external trigger	-
14	PB2/AIN2 [TIM1_CH3N]	I/O	X	X	X	HS	O3	X	X	Port B2	Analog input 2/Timer 1 - inverted channel 3	-
15	PB1/AIN1 [TIM1_CH2N]	I/O	X	X	X	HS	O3	X	X	Port B1	Analog input 1/Timer 1 - inverted channel 2	-
16	PB0/AIN0 [TIM1_CH1N]	I/O	X	X	X	HS	O3	X	X	Port B0	Analog input 0/Timer 1 - inverted channel 1	-
17	PE5/SPI_NSS	I/O	X	X	X	HS	O3	X	X	Port E5	SPI master/slave select	-
18	PC1/TIM1_CH1/ UART1_CK	I/O	X	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1 UART1 clock	-
19	PC2/TIM1_CH2	I/O	X	X	X	HS	O3	X	X	Port C2	Timer 1- channel 2	-
20	PC3/TIM1_CH3	I/O	X	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	-

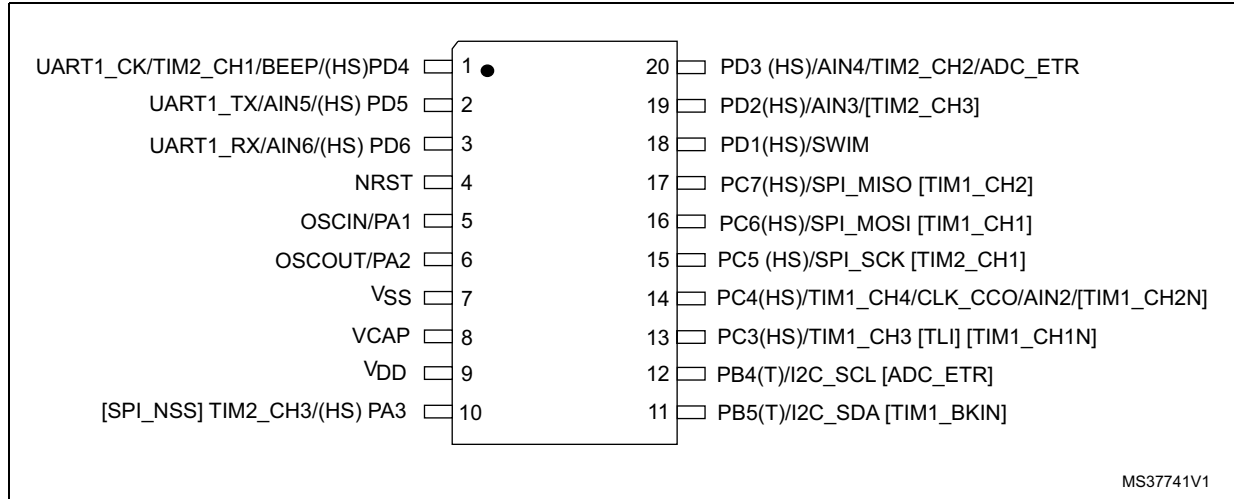
Table 5. STM8S003K3 descriptions (continued)

LQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink <sup>(1)</sup>	Speed	OD	PP			
21	PC4/TIM1_CH4/CLK_CCO	I/O	X	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4/configurable clock output	-
22	PC5/SPI_SCK	I/O	X	X	X	HS	O3	X	X	Port C5	SPI clock	-
23	PC6/SPI_MOSI	I/O	X	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	-
24	PC7/SPI_MISO	I/O	X	X	X	HS	O3	X	X	Port C7	SPI master in/slave out	-
25	PD0/[TIM1_BKIN [CLK_CCO]]	I/O	X	X	X	HS	O3	X	X	Port D0	Timer 1 - break input	Configurable clock output [AFR5]
26	PD1/SWIM <sup>(4)</sup>	I/O	X	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
27	PD2 [TIM2_CH3]	I/O	X	X	X	HS	O3	X	X	Port D2	-	Timer 2 - channel 3 [AFR1]
28	PD3/TIM2_CH2 [ADC_ETR]	I/O	X	X	X	HS	O3	X	X	Port D3	Timer 2 - channel 2/ADC external trigger	-
29	PD4/BEEP/TIM2_CH1	I/O	X	X	X	HS	O3	X	X	Port D4	Timer 2 - channel 1/BEEP output	-
30	PD5/ UART1_TX	I/O	X	X	X	HS	O3	X	X	Port D5	UART1 data transmit	-
31	PD6/ UART1_RX	I/O	X	X	X	HS	O3	X	X	Port D6	UART1 data receive	-
32	PD7/TLI [TIM1_CH4]	I/O	X	X	X	HS	O3	X	X	Port D7	Top level interrupt	Timer 1 - channel 4 [AFR6]

1. I/O pins used simultaneously for high-current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings given in [Section 9: Electrical characteristics](#).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, "T" defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to  $V_{DD}$  are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after the internal reset release.

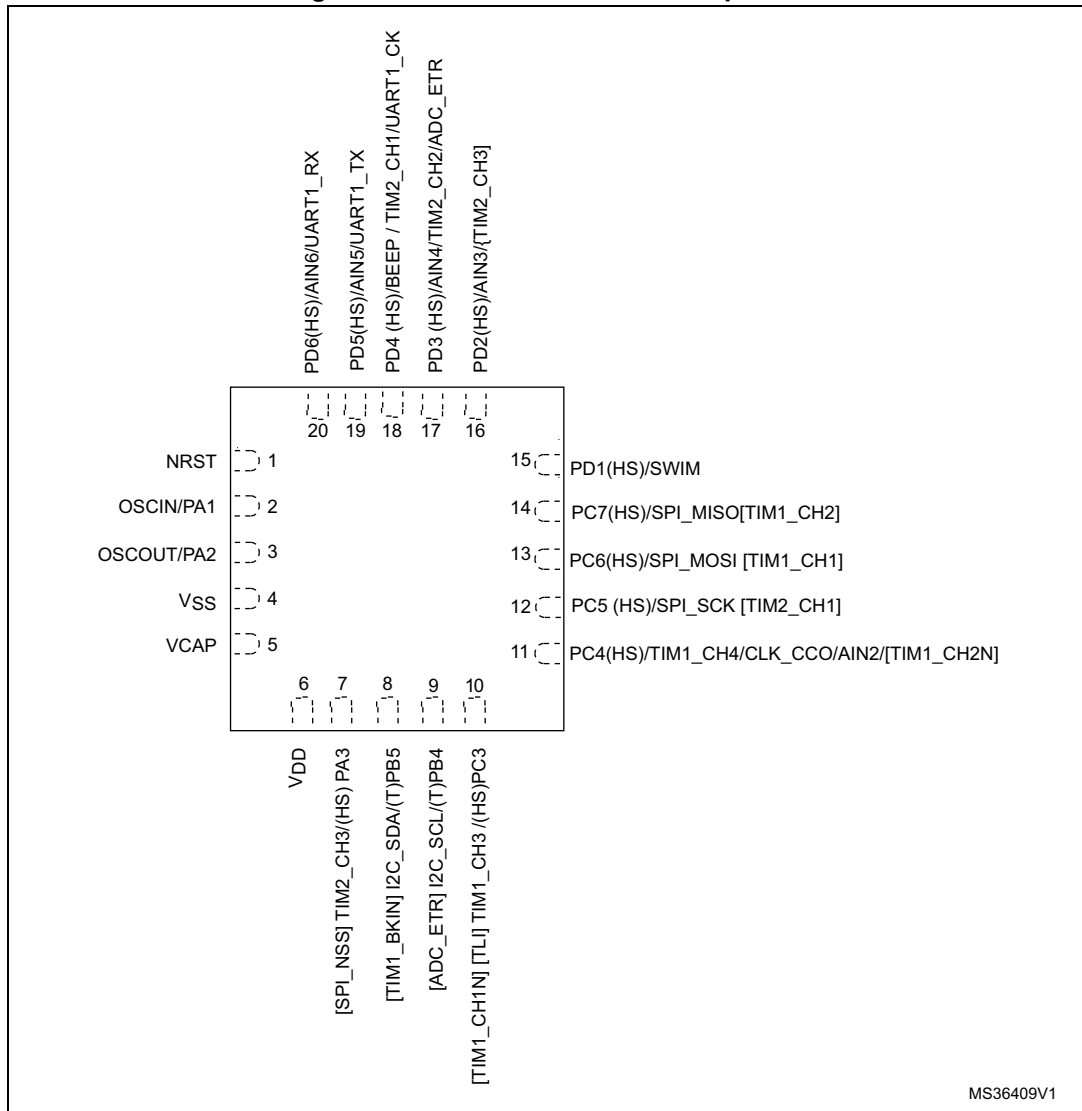
## 5.2 STM8S003F3 TSSOP20/UFQFPN20 pinout and pin description

Figure 4. STM8S003F3 TSSOP20 pinout



1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to VDD not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 5. STM8S003F3 UFQFPN20 pinout



MS36409V1

1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to VDD not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. STM8S003F3 pin description

Pin no.		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
TSSOP20	UFQFPN20			floating	wpu	Ext. interr.	High sink <sup>(1)</sup>	Speed	OD	PP			
1	18	PD4/ BEEP/ TIM2_CH1/ UART1_CK	I/O	X	X	X	HS	O3	X	X	Port D4	Timer 2 - channel 1/BEEP output/ UART1 clock	-
2	19	PD5/ AIN5/ UART1_TX	I/O	X	X	X	HS	O3	X	X	Port D5	Analog input 5/ UART1 data transmit	-
3	20	PD6/ AIN6/ UART1_RX	I/O	X	X	X	HS	O3	X	X	Port D6	Analog input 6/ UART1 data receive	-
4	1	NRST	I/O	-	X	-	-	-	-	-	Reset		-
5	2	PA1/ OSCIN <sup>(2)</sup>	I/O	X	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	3	PA2/ OSCOUT	I/O	X	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
7	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
9	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	7	PA3/ TIM2_CH3 [SPI_NSS]	I/O	X	X	X	HS	O3	X	X	Port A3	Timer 2 channel 3	SPI master/ slave select [AFR1]
11	8	PB5/ I2C_SDA [TIM1_BKIN]	I/O	X	-	X	-	O1	T <sup>(3)</sup>	-	Port B5	I2C data	Timer 1 - break input [AFR4]
12	9	PB4/ I2C_SCL	I/O	X	-	X	-	O1	T <sup>(3)</sup>	-	Port B4	I2C clock	ADC external trigger [AFR4]
13	10	PC3/ TIM1_CH3 [TLI] [TIM1_CH1N]	I/O	X	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 - inverted channel 1 [AFR7]

Table 6. STM8S003F3 pin description (continued)

Pin no.		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
TSSOP20	UFQFPN20			floating	wpu	Ext. interr.	High sink <sup>(1)</sup>	Speed	OD	PP			
14	11	PC4/CLK_CCO/ TIM1_ CH4/AIN2/ [TIM1_ CH2N]	I/O	X	X	X	HS	O3	X	X	Port C4	Configurable clock output/Timer 1 - channel 4/Analog input 2	Timer 1 - inverted channel 2 [AFR7]
15	12	PC5/ SPI_SCK [TIM2_ CH1]	I/O	X	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 2 - channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_ CH1]	I/O	X	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	Timer 1 - channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_ CH2]	I/O	X	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 - channel 2 [AFR0]
18	15	PD1/ SWIM <sup>(4)</sup>	I/O	X	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
19	16	PD2/AIN3/ [TIM2_ CH3]	I/O	X	X	X	HS	O3	X	X	Port D2	Analog input 3	Timer 2 - channel 3 [AFR1]
20	17	PD3/ AIN4/ TIM2_ CH2/ ADC_ ETR	I/O	X	X	X	HS	O3	X	X	Port D3	Analog input 4/ Timer 2 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings.
2. When the MCU is in halt/active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if halt/active-halt is used in the application.
3. In the open-drain output column, "T" defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

### 5.3 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to [Section 8: Option bytes](#). When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

## 6 Memory and register map

### 6.1 Memory map

Figure 6. Memory map

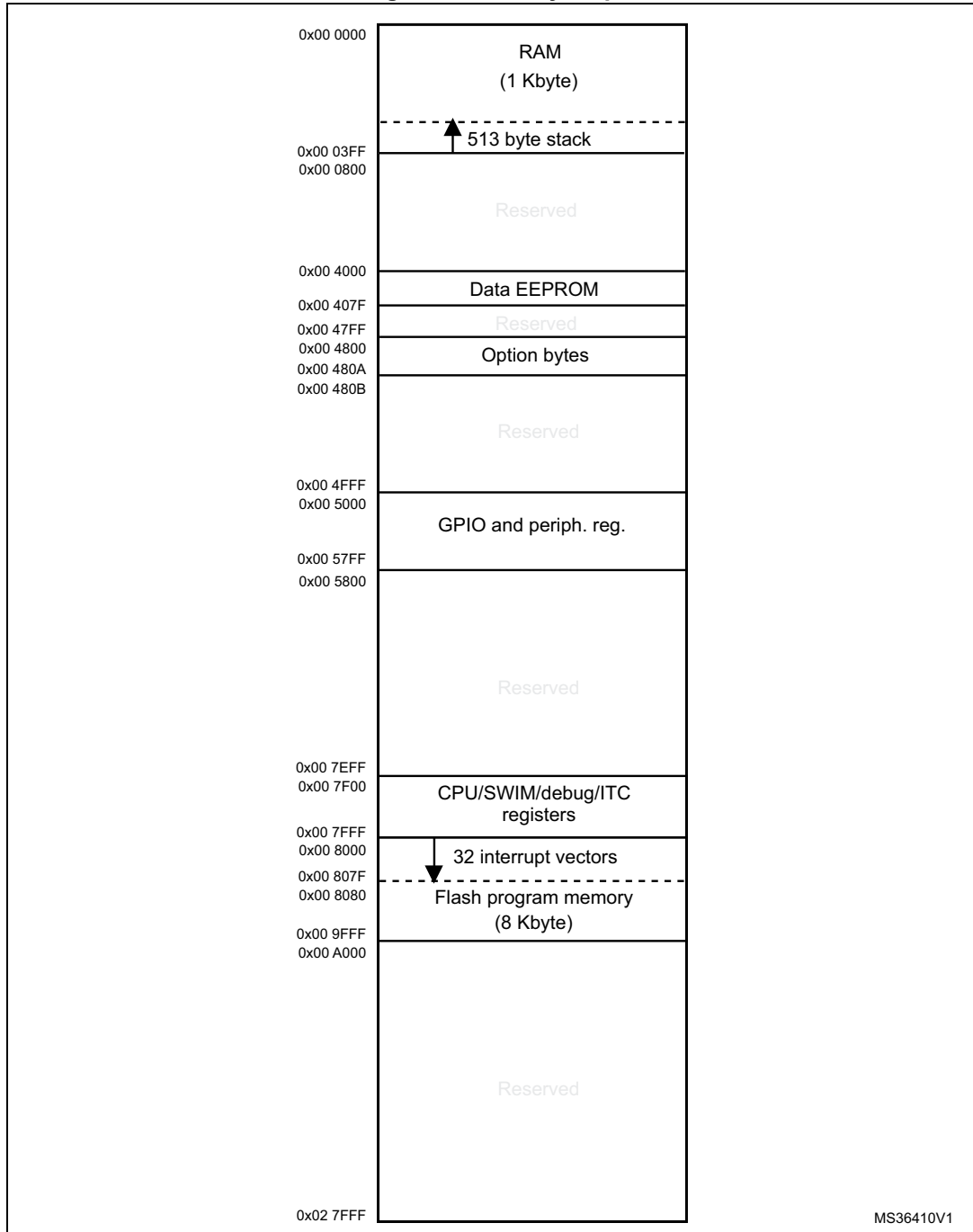


Table 7 lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

**Table 7. Flash, Data EEPROM and RAM boundary addresses**

Memory area	Size (byte)	Start address	End address
Flash program memory	8 K	0x00 8000	0x00 9FFF
RAM	1 K	0x00 0000	0x00 03FF
Data EEPROM	128	0x00 4000	0x00 407F

## 6.2 Register map

### 6.2.1 I/O port hardware register map

**Table 8. I/O port hardware register map**

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX <sup>(1)</sup>
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX <sup>(1)</sup>
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX <sup>(1)</sup>
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX <sup>(1)</sup>
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX <sup>(1)</sup>
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX <sup>(1)</sup>
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

1. Depends on the external circuitry.

## 6.2.2 General hardware register map

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5059	Reserved area (60 byte)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH_FPR	Flash protection register	0x00
0x00 505E		FLASH_NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH_IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 byte)			
0x00 5062	Flash	FLASH_PUKR	Flash Program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH_DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 byte)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 byte)			
0x00 50B3	RST	RST_SR	Reset status register	0xFF <sup>(1)</sup>
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xFF
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB	Reserved area (1 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50CC	CLK	CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 byte)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX <sup>(2)</sup>
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 byte)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCR	SPI Rx CRC register	0x00
0x00 5207		SPI_TXCR	SPI Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I <sup>2</sup> C	I2C_CR1	I <sup>2</sup> C control register 1	0x00
0x00 5211		I2C_CR2	I <sup>2</sup> C control register 2	0x00
0x00 5212		I2C_FREQR	I <sup>2</sup> C frequency register	0x00
0x00 5213		I2C_OARL	I <sup>2</sup> C own address register low	0x00
0x00 5214		I2C_OARH	I <sup>2</sup> C own address register high	0x00
0x00 5215		Reserved		

**Table 9. General hardware register map (continued)**

Address	Block	Register label	Register name	Reset status
0x00 5216	I <sup>2</sup> C	I2C_DR	I <sup>2</sup> C data register	0x00
0x00 5217		I2C_SR1	I <sup>2</sup> C status register 1	0x00
0x00 5218		I2C_SR2	I <sup>2</sup> C status register 2	0x00
0x00 5219		I2C_SR3	I <sup>2</sup> C status register 3	0x00
0x00 521A		I2C_ITR	I <sup>2</sup> C interrupt control register	0x00
0x00 521B		I2C_CCRL	I <sup>2</sup> C clock control register low	0x00
0x00 521C		I2C_CCRH	I <sup>2</sup> C clock control register high	0x00
0x00 521D		I2C_TRISER	I <sup>2</sup> C TRISE register	0x02
0x00 521E		I2C_PECR	I <sup>2</sup> C packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 byte)			
0x00 5230	UART1	UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xFF
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235		UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00523F	Reserved area (21 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E	TIM1_DTR	TIM1 dead-time register	0x00	
0x00 526F	TIM1_OISR	TIM1 output idle state register	0x00	
0x00 5270 to 0x00 52FF	Reserved area (147 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		Reserved		
0x00 5302		Reserved		
0x00 5303		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5304		TIM2_SR1	TIM2 status register 1	0x00
0x00 5305		TIM2_SR2	TIM2 status register 2	0x00
0x00 5306		TIM2_EGR	TIM2 event generation register	0x00
0x00 5307		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5308		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5309		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 530A		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 530B		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 530E		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530F		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 5310		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5311		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5312		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5313		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5314		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5315		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5316		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5317 to 0x00 533F	Reserved area (43 byte)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		Reserved		
0x00 5342		Reserved		
0x00 5343		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5344		TIM4_SR	TIM4 status register	0x00
0x00 5345		TIM4_EGR	TIM4 event generation register	0x00
0x00 5346		TIM4_CNTR	TIM4 counter	0x00
0x00 5347		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5348		TIM4_ARR	TIM4 auto-reload register	0xFF

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5349 to 0x00 53DF	Reserved area (153 byte)			
0x00 53E0 to 0x00 53F3	ADC1	ADC_DBxR	ADC data buffer registers	0x00
0x00 53F4 to 0x00 53FF	Reserved area (12 byte)			
0x00 5400	ADC1	ADC_CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC_HTRH	ADC high threshold register high	0x03
0x00 5409		ADC_HTRL	ADC high threshold register low	0xFF
0x00 540A		ADC_LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC_AWSRH	ADC analog watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC analog watchdog status register low	0x00
0x00 540E		ADC_AWCRH	ADC analog watchdog control register high	0x00
0x00 540F		ADC_AWCRL	ADC analog watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 byte)			

1. Depends on the previous reset source.
2. Write only register.

6.2.3 CPU/SWIM/debug module/interrupt controller registers

Table 10. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register Label	Register Name	Reset Status	
0x00 7F00	CPU <sup>(1)</sup>	A	Accumulator	0x00	
0x00 7F01		PCE	Program counter extended	0x00	
0x00 7F02		PCH	Program counter high	0x00	
0x00 7F03		PCL	Program counter low	0x00	
0x00 7F04		XH	X index register high	0x00	
0x00 7F05		XL	X index register low	0x00	
0x00 7F06		YH	Y index register high	0x00	
0x00 7F07		YL	Y index register low	0x00	
0x00 7F08		SPH	Stack pointer high	0x03	
0x00 7F09		SPL	Stack pointer low	0xFF	
0x00 7F0A		CCR	Condition code register	0x28	
0x00 7F0B to 0x00 7F5F		Reserved area (85 byte)			
0x00 7F60		CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF	
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF	
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF	
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF	
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF	
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF	
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF	
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF	
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)				
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00	
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)				

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register Label	Register Name	Reset Status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F		Reserved area (5 byte)		

1. Accessible by debug module only